REMARKS

In response to the above-identified Office Action, Applicant amends the application and seeks reconsideration thereof. In this response Applicant did not amend, cancel or add any claim. Accordingly, Claims 1-4 are pending.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

I. Drawings

It is asserted in the Office Action that the drawings are objected to because Figure 1 should be designed by a legend such as –Prior Art- to illustrate what is old. Applicants have amended Figure 1 in order to overcome the objections. Withdrawal of this objection is respectfully requested.

II. Specification

The title has been changed to clearly indicate the invention to which the claims are directed. Withdrawal of this objection is respectfully requested.

The Abstract of the Disclosure has been corrected to conform to MPEP § 608.01(b). Withdrawal of this objection is respectfully requested.

Changes also have been made to both the Prior Art of the Invention section and the Preferred Embodiment of the Invention section to reflect appropriate corrections to typographical errors.

III. Claims Rejected Under 35 U.S.C. §103(a)

The Office rejected Claims 1 and 4 under 35 U.S.C.§103(a) as being unpatentable over Nakayama et al., U.S. Patent No. 6,242,787 (hereinafter "Nakayama"), in view of Applicant Admitted Prior Art (hereinafter "AAPA"). Applicant respectfully disagrees.

In order to render a claim obvious, the replied upon reference must teach or suggest every limitation of the claim such that the invention as a whole would have been obvious at the time the invention was made to one skilled in the art.

Nakayama discloses a LDMOS device that includes a P-type first well and a N-type second well formed in the N-type semiconductor layer to make a double–well

structure and to establish LDMOS (Nakayama , column 4, lines 32-35). The second well has a source region, a channel region and a drain region therein and a gate electrode is disposed on the channel region so that the second well serves as a drift region. (Nakayama , column 12, lines 28-57). In the case that a reverse voltage is applied to the drain region, the source and the semiconductor layer is set to be equal in electric potential to each other (Nakayama, column 3, lines 36-43). Additionally, a parasitic transistor is formed among the second well, the first well and the semiconductor layer to establish a current-carrying path. (Nakayama, column 3, lines 43-46). This current–carrying path can prevent the breakdown of the elements at the channel formation portions. (Nakayama, column 4, lines 6-7).

Applicant's claims are directed to a LDMOSFET device that includes a trench type sinker and a second conductive type LDD area. Applicant's claim 1 states the limitation that "a sinker as the first conductive type provided as a column shape of a trench structure for dividing into two source areas by a piercing through the source area, and connected to the semiconductor layer." In other words, the sinker divides the source area into two source areas. Applicant is unable to find that Nakayama teaches, suggests or discloses "a sinker as the first conductive type provided as a column shape of a trench structure for dividing into two source areas." Contrary to the Office's opinion, the source area in Nakayama is not divided into two source areas by P^+ and P regions. In fact, the P^+ and P regions only form part of the N^+ source area as indicated in Figure 8 of Nakayama and do not divide the N^+ source area. Thus, Nakayama does not teach or suggest the use of a sinker in the source area to divide the source area into two source areas.

Applicant's Claim 1 further recites the limitations of "a channel layer as a second conductive type laterally diffused from the field area to a width containing both sides of the gate electrode, and formed on the surface of the semiconductor layer" and "an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode." The Office admits that "Nakayama et al. do not teach in the embodiment of figure 8 a channel layer formed from the field area and an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode." The Office further admits that "Nakayama et al. teach in the embodiment of figure 4 a channel layer N

formed from the field area 23 (the channel layer N of LDMOS is formed from the left field area 23)." The channel layer in Nakayama does not form from the field area to a width containing both sides of the gate electrode. In fact, the channel layer in Nakayama is formed away from the source and the gate electrode. The Office further admits that "Nakayama et al. teach in the embodiment of figure 4 a channel layer N formed from the field area 23 (the channel layer N of LDMOS is formed from the left field area 23)." In other words, according to the Office, Nakayama teaches in the embodiment of figure 4 a channel layer N formed strictly within the field area. Thus, it would not have been obvious to a person of ordinary skill in the art at the time the invention was made to form the channel layer from the field area and to use an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode.

Claim 4 depends from Claim 1. As Claim 1, the independent claim, is patentable in view of Nakayama, Applicants respectfully submit for at least the same reasons, Claim 4, the dependent claim is also patentable in view of Nakayama.

Because the combination of AAPA and Nakayama does not teach or suggest every limitation of claims 1 and 4, the Applicant's invention as a whole would not have been obvious at the time the invention was made to one skilled in the art. Accordingly, Applicant respectfully requests withdrawal of the rejection of Claims 1 and 4 under 35 U.S.C. § 103(a).

The Office also rejected Claims 2 and 3 under 35 U.S.C. §103(a) as being unpatentable over Nakayama and AAPA, and further in view of Tihanyi, U.S. Patent No. 6,242,787 (hereinafter "Tihanyi"). Applicant respectfully disagrees.

Applicant's Claims 2 and 3 are dependent upon base Claim 1. Applicant's Claim 1 recites the limitation ""a sinker as the first conductive type provided as a column shape of a trench structure for dividing into two source areas by a piercing through the source area, and connected to the semiconductor layer." Tihanyi, on the other hand, teaches the formation of the trenches within an epitaxial layer and "the trenches being organized in lines and rows between the source terminal region and the drain terminal region" (Tihanyi, column 1, lines 53-59). In fact, Tihanyi teaches away from using a trench structure in the source area by disclosing formation of trench structure along the drain area such that "the drain electrode essentially being disposed in the center of such

a structure" (Tihanyi, column 2, lines 33-36). Thus, Tihanyi neither teaches, suggests or motivates towards using a trench structure for a sinker in the source area. Accordingly, Applicant respectfully requests withdrawal of the rejection of Claims 2 and 3 under 35 U.S.C. § 103(a).

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/9, 2002

Eric S. Hyman, Reg. No. 30,139

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 9, 2002.

Nadya Gordon 12/9/02

Nadya Gordon *December 9, 2002*

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 2, starting on line 11, the paragraph is amended as follows:

As shown in Fig. 1, in the LDMOS based on the conventional technique, the MOSFET is made on a wafer 13 which is constructed by P^- epitaxy layer 12 on P^+ substrate 11. What this is different from a general MOSFET device manufacturing process is that an overall lower part of the substrate is used as common source electrode [21] 22 by forming a P^+ sinker 14 on a source side of the wafer 13 and connecting with a P^+ substrate 11.

On page 8, starting on line 24, the paragraph is amended as follows:

Fig. 3 is a structural sectional view of an HF power device taken along the line A-A′ of Fig. 2, and it is constructed by a P^- semiconductor layer 31b expitaxial-grown on a P^+ substrate 31a; a field oxide film 41 formed by a trench structure on one side of the P^- semiconductor layer 31b; a polysilicon 43a formed on a given surface of the P^- semiconductor layer [31a] 31b and gate electrode 44 of a tungsten silicide 43b laminating structure; a channel layer 46 laterally diffused from the field oxide film 41 to both sides of the gate electrode 44, and formed on the surface of the P^- semiconductor layer 31b; an N^+ source area 47 formed within the channel layer 46 between one side of the gate electrode 44 and the field oxide film 41; an N^+ drain area 48 formed on the surface of the P^- semiconductor layer 31b with a given interval from another side of the gate electrode 44; a P^+ sinker 37 provided as a column shape of a trench structure for dividing into two source areas by a piercing through the N^+ source area 47, and connected to the P^+ substrate 31a; an N^- LDD area 45 formed on the surface of the P^- semiconductor layer 31b between the N^+ drain area 48 and the gate electrode 44; source electrode 51 contacted with the N^+ source area 47 divided into two source areas and electrically coupled with the P^+ substrate 31a through the P^+ sinker 37; and drain electrode 52 contacted with the N^+ drain area 48.

On page 9, starting on line 23, the paragraph is amended as follows:

The P^- sinker 37 includes the P^+ polysilicon column 36b buried into one or numerous trenches formed by etching the P^- semiconductor layer 31b by a given depth and the neighborhood of the trench, namely, a P' coping layer [37a] 37b provided by a doping on a lower part and a side wall thereof.

IN THE ABSTRACT

The Abstract is amended as follows:

A device structure of a LDMOSFET has a trench type sinker formed using a trench process. A semiconductor layer of a first conductive type is formed within the device structure. A field area is formed in a trench structure on one side of the semiconductor layer and a gate electrode is formed on a given surface of the semiconductor layer. A channel layer of a second conductive type is formed by laterally diffusion from the field area to a width containing both sides of the gate electrode. The source area of LDMOS is electrically connected with the substrate through the sinker. By a piercing through the source area, the sinker divides the source area into two source areas. This division reduces the parasitic resistance as well as parasitic capacitance. In addition, the device structure eliminates the need for high temperature diffusion process and reduces lateral diffusion of the sinker. [A device structure of a LDMOSFET has a trench type sinker formed using a trench process. A semiconductor layer of a first conductive type is formed within the device structure. A field area is formed in a trench structure on one side of the semiconductor layer and a gate electrode is formed on a given surface of the semiconductor layer. A channel layer of a second conductive type is formed by laterally diffusion from the field area to a width containing both sides of the gate electrode. The source area of LDMOS is electrically connected with the substrate through the sinker. By a piercing through the source area, the sinker divides the source area into two source areas. This division reduces the parasitic resistance as well as parasitic capacitance. In addition, the device structure eliminates the need for high temperature diffusion process and reduces lateral diffusion of the sinker.]

ABSTRACT OF THE DISCLOSURE

A device structure of a LDMOSFET has a trench type sinker formed using a trench process. A semiconductor layer of a first conductive type is formed within the device structure. A field area is formed in a trench structure on one side of the semiconductor layer and a gate electrode is formed on a given surface of the semiconductor layer. A channel layer of a second conductive type is formed by laterally diffusion from the field area to a width containing both sides of the gate electrode. The source area of LDMOS is electrically connected with the substrate through the sinker. By a piercing through the source area, the sinker divides the source area into two source areas. This division reduces the parasitic resistance as well as parasitic capacitance. In addition, the device structure eliminates the need for high temperature diffusion process and reduces lateral diffusion of the sinker.